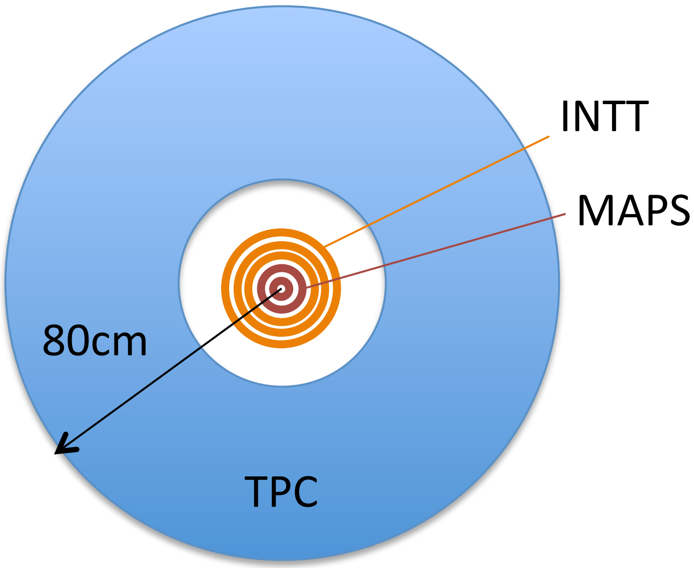
# Intermediate Silicon Tracker Overview

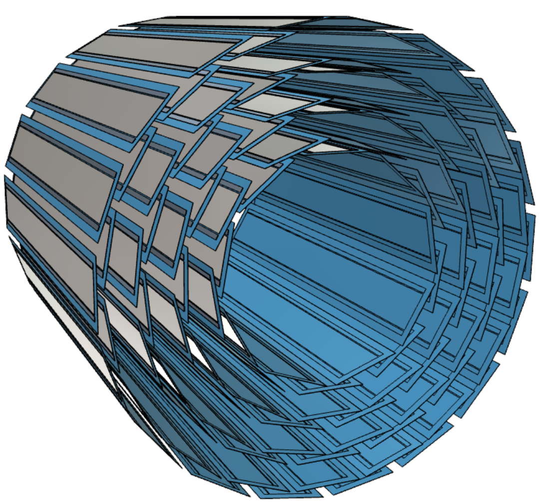
RIKEN/RBRC
Itaru Nakagawa

# Quick Overview of Intermediate Silicon Tracker (INTT)

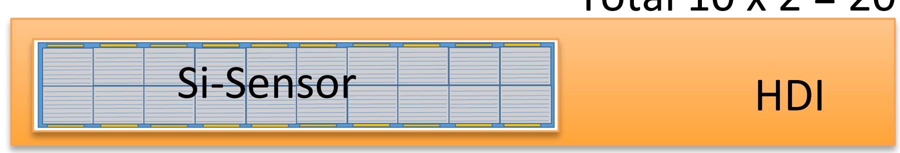



| | R [cm] | # of Ladders |
|---|---|---|
| MAPS | 2.3 | |
| | 3.1 | |
| | 3.9 | |
| **INTT** | **6** | 18 |
| | **8** | 24 |
| | **10** | 30 |
| | **12** | 36 |
| TPC | 30 ~ 80 | |

Total Number of Ladders=108



Total 10 x 2 = 20 cells/ladder

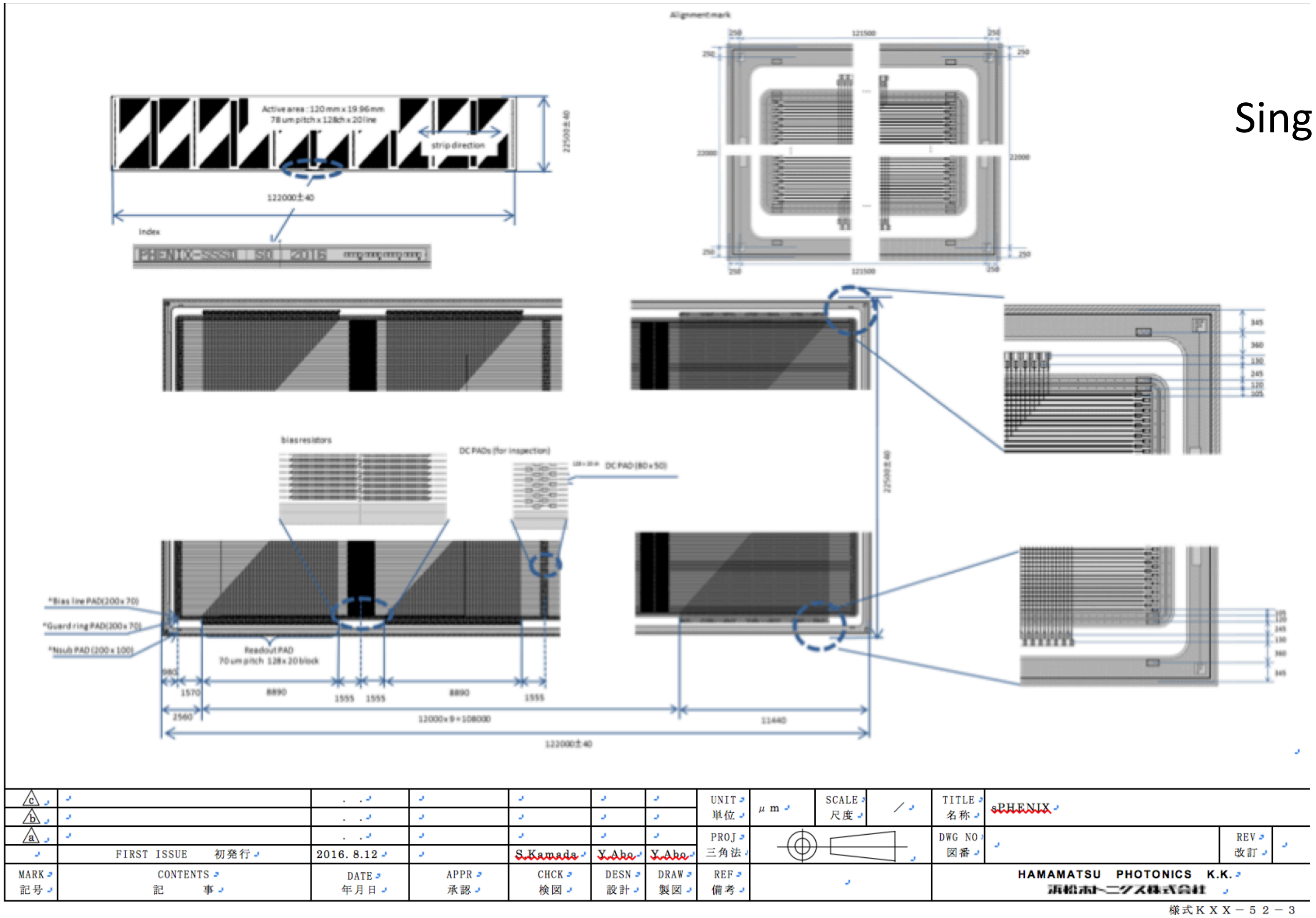


# Project Scope (Role of INTT)

1. DCA measurements
   - Connect MAPS tracklets and TPC track
   - Reduce backgrounds in DCA
2. Pile-up
   - Improve track finding efficiency in central Au-Au
3. TPC Calibration
   - Identify track position for the space-time calibration of TPC

Boundary condition:
- Material budgets to be as smallest as possible.
- Minimum technical risk to be in time for day-1.

# Technology Choice



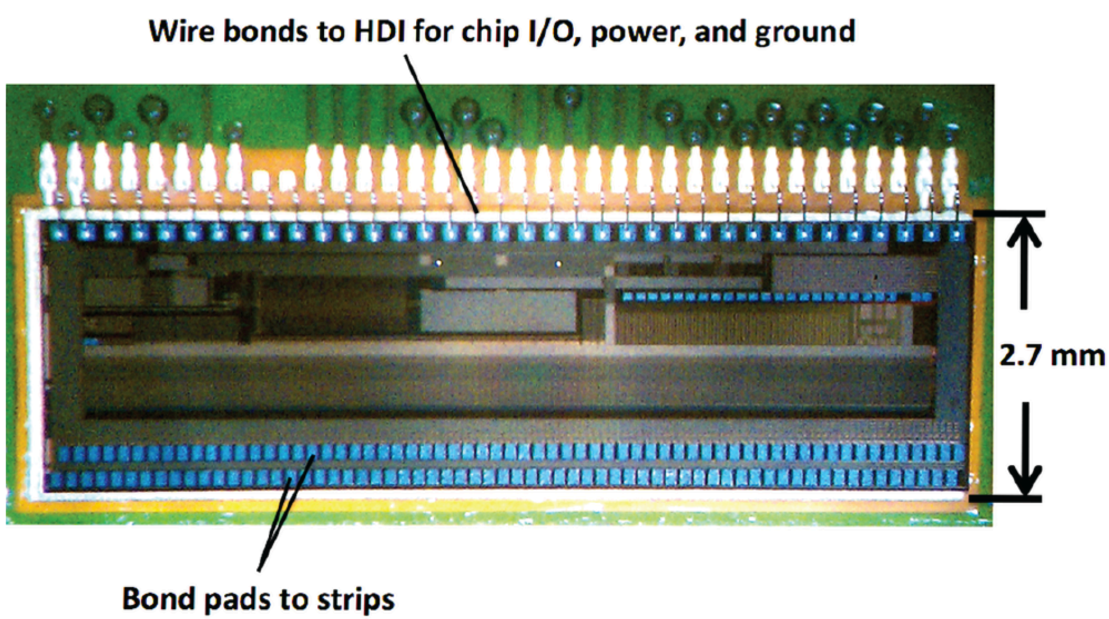

Single sided silicon strip sensors
(Hamamatsu Co.)


Challenge to develop thinner detector to reduce material budgets.
Standard 320μm -> 200μm?

# FPHX Chip

FVTX Silicon Module for PHENIX


- Developed for FVTX and proven to work well
- Low power consumption



# FPHX Power Consumption

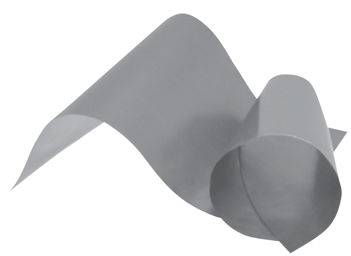
| Specification | FPHX |
|---|---|
| ADC/channel | 3 bits |
| Power Consumption | 64 mW |
| Cooling | Air or Solid* |

**Panasonic** “PGS” Graphite Sheets

### “PGS” Graphite Sheets

Type: **EYG**

“PGS (Pyrolytic Graphite Sheet)” is a thermal interface material which is very thin, synthetically made, has high thermal conductivity, and is made from a higly oriented graphite polymer film. It is ideal for providing thermal management/heat-sinking in limited spaces or to provide supplemental



**Features**

- Excellent thermal conductivity : 700 to 1950 W/(m·K)
  (2 to 5 times as high as copper, 3 to 8 time as high as aluminum)

## Material Budget of PHENIX VTX

| Current VTX Stripixel Stave | |
|---|---|
| Carbon Face Sheet | 0.43% |
| Al Tube (square 0.014" walls) | 0.45% |
| Novec | 0.39% |
| Carbon Foam | 0.20% |
| **Total** | **1.47%** |

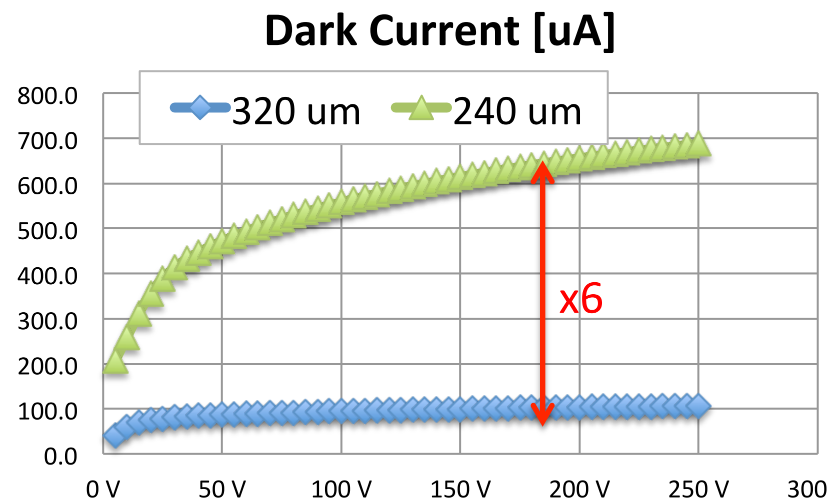
| VTX Stave w/ Stainless steel & Carbon Foam | |
|---|---|
| Carbon Face Sheet | 0.43% |
| Stainless Steel Tube (3/16" ID .007" walls) | 0.40% |
| Novec | 0.39% |
| Carbon Foam | 0.20% |
| **Total** | **1.42%** |

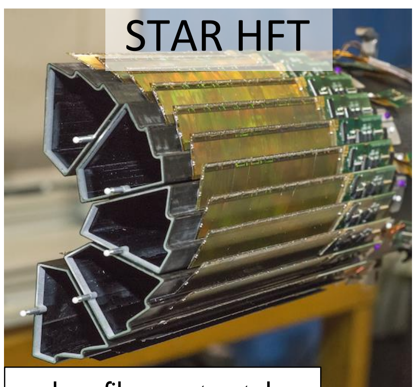
| VTX Stave w/ Carbon-loaded PEEK | |
|---|---|
| Carbon Face Sheet | 0.43% |
| Novec (Same volume as current stave) | 0.39% |
| Carbon Loaded PEEK (L_rad=28 cm) | 1.04% |
| **Total** | **1.86%** |

| $X_{rad}$ [μm] | $X_{rad}/X_0$ [%] |
|---|---|
| 100 - 500 | 0.05 – 0.25 |

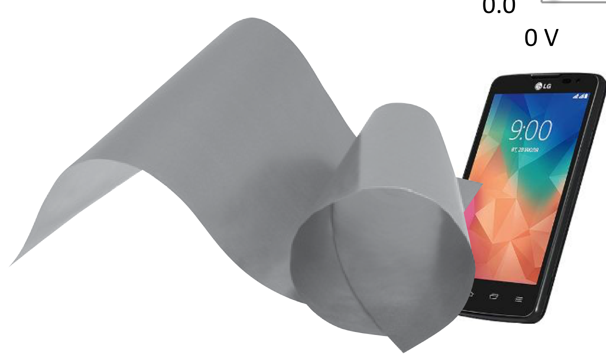
# Technical Challenge

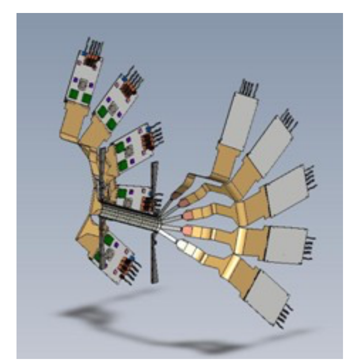
- Thinner Silicon Sensor
  - Trade off of S/N ratio
- Air/Solid Coolings



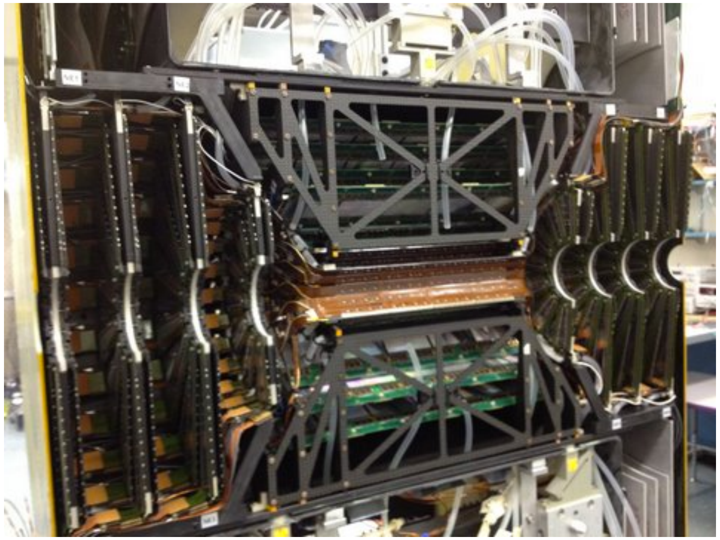
carbon fiber sector tubes
(~ 200 μm thick)

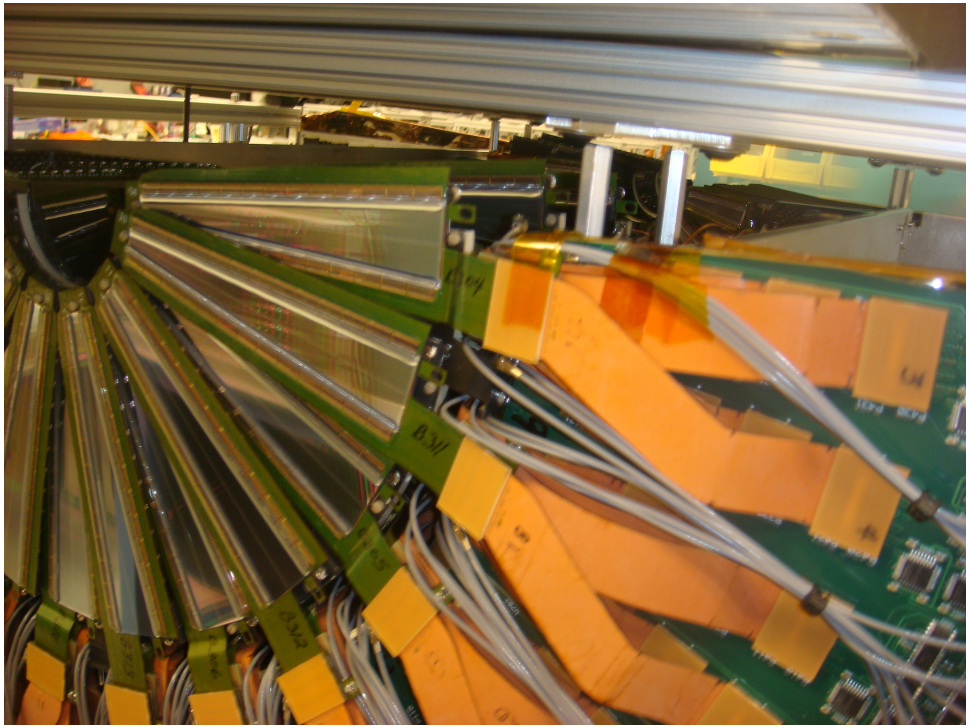


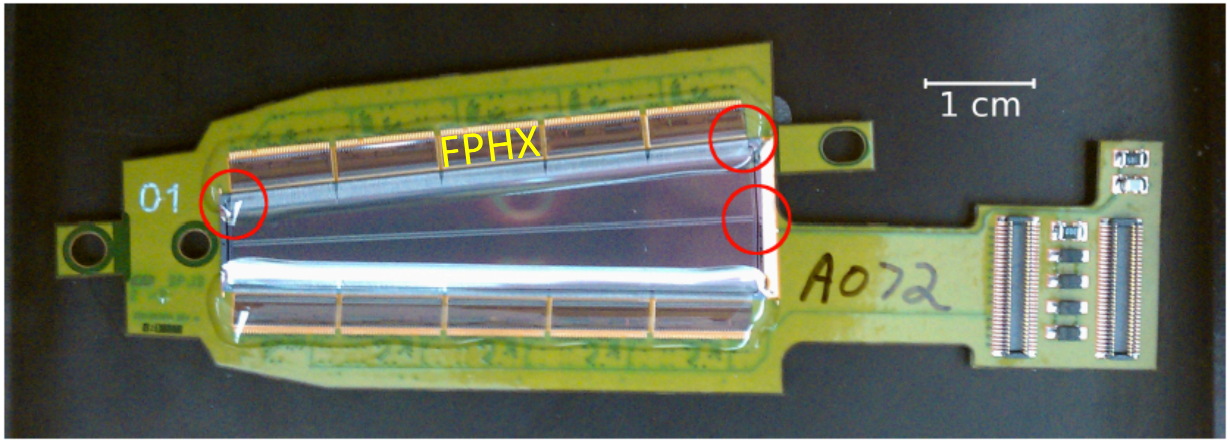


- Adaption of FVTX Electronics to INTT.

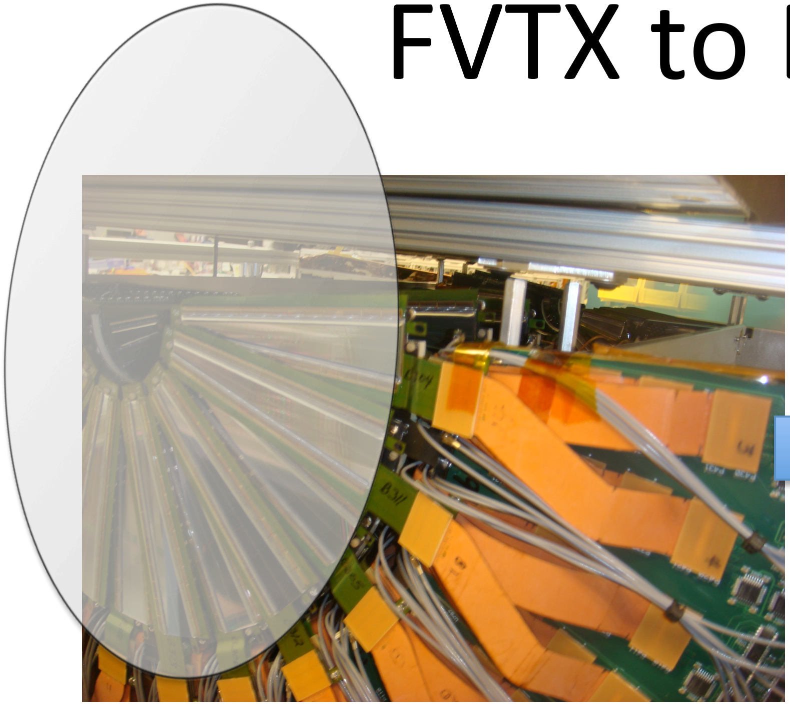
# FVTX Detector



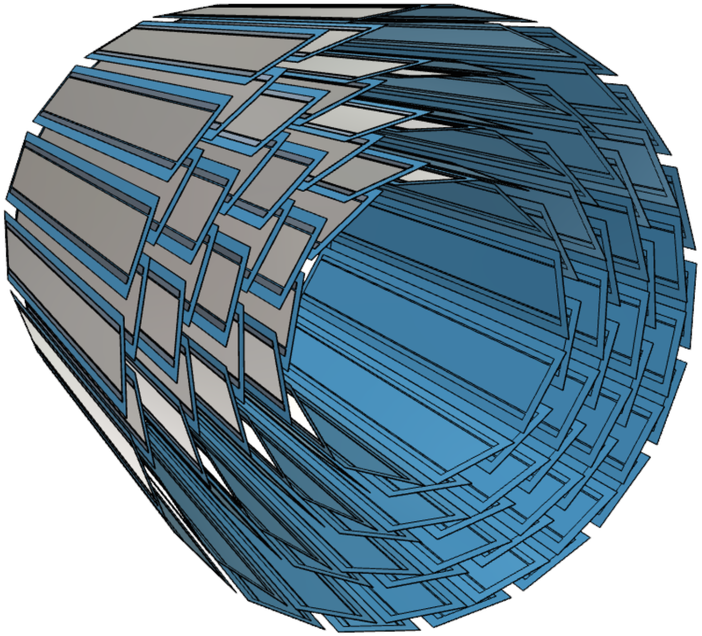




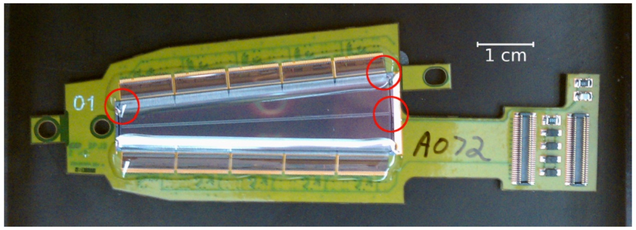
# FVTX to Barrel Tracker



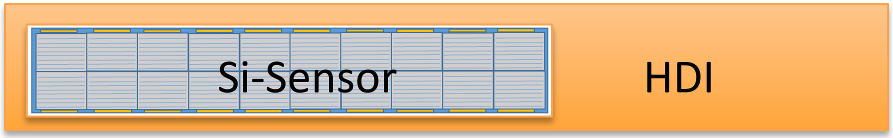
Disk



Barrel



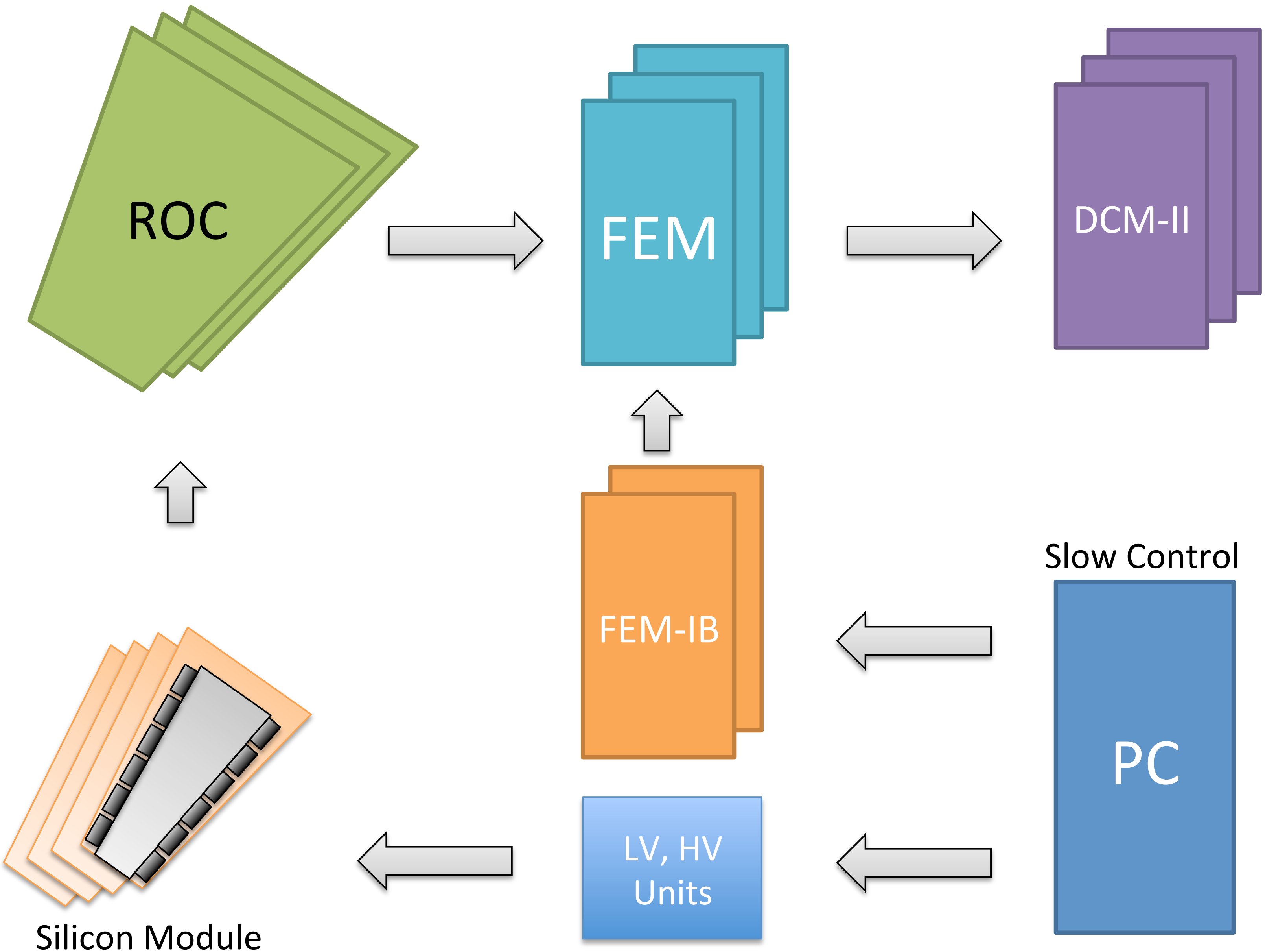

Trapezoid



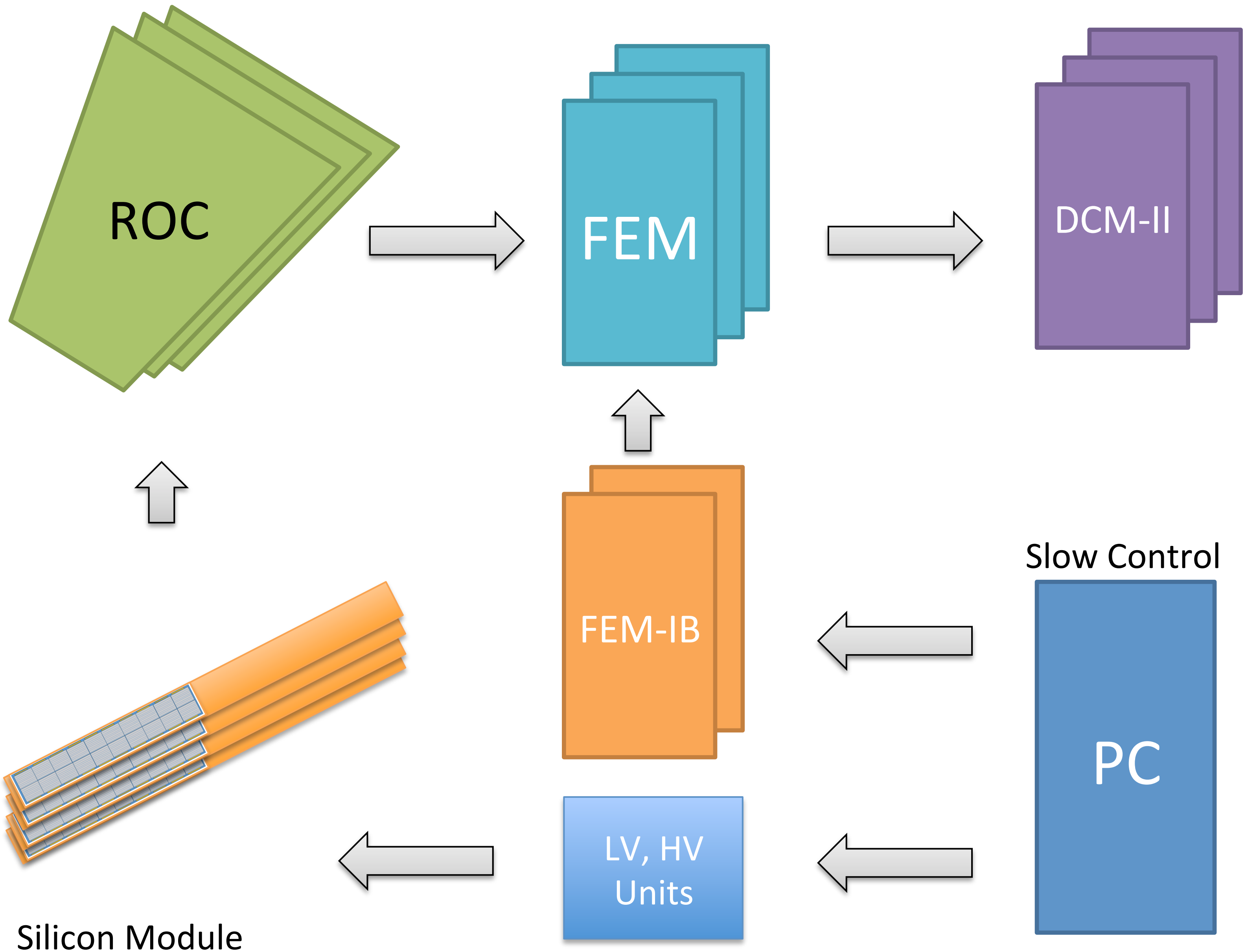

Rectangular

Geometry needs to be changed, but **electrical design** could be the same.

# FVTX System


ROC
FEM
DCM-II
FEM-IB
Slow Control
PC
LV, HV
Units
Silicon Module

# INTT System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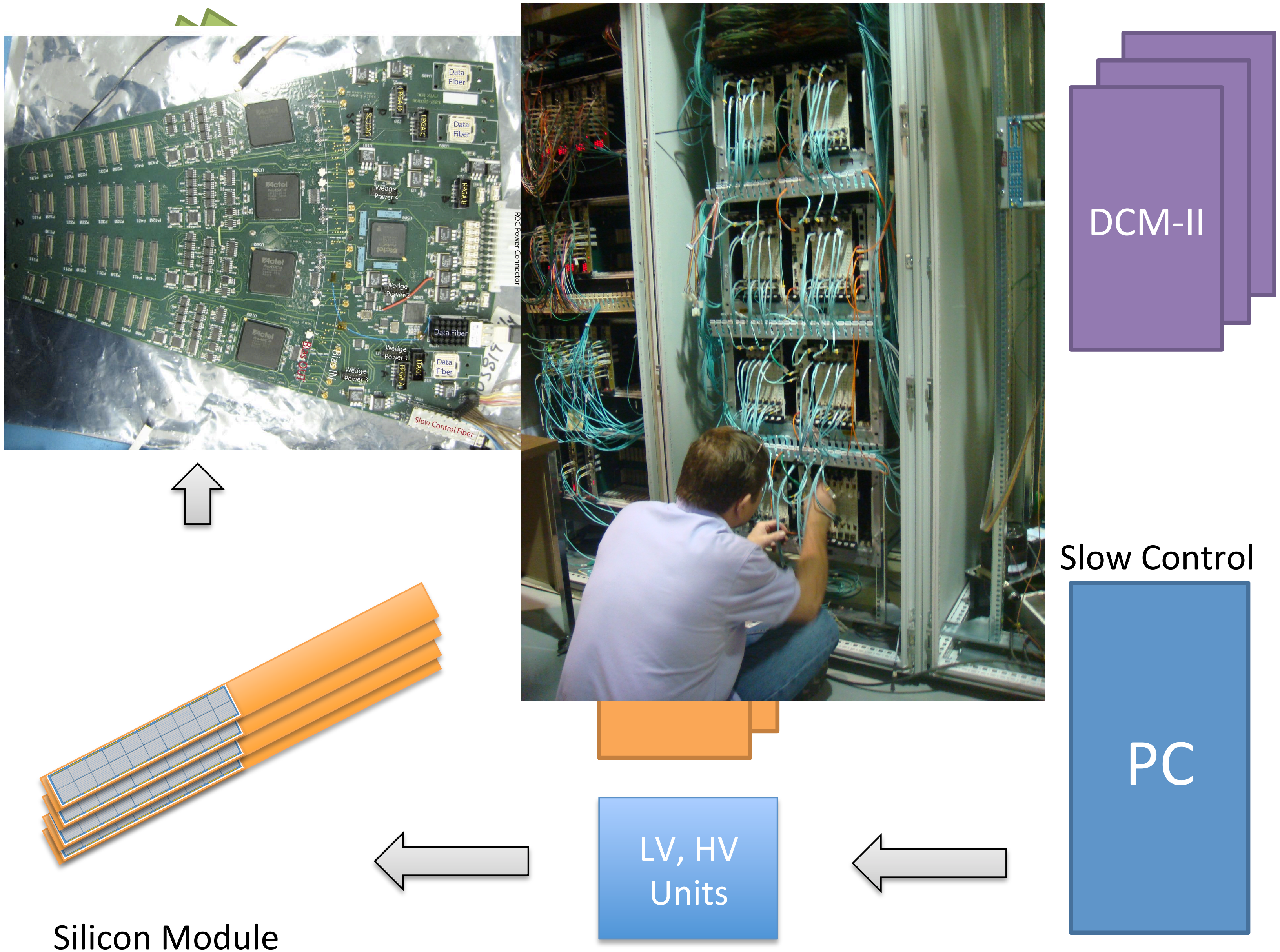
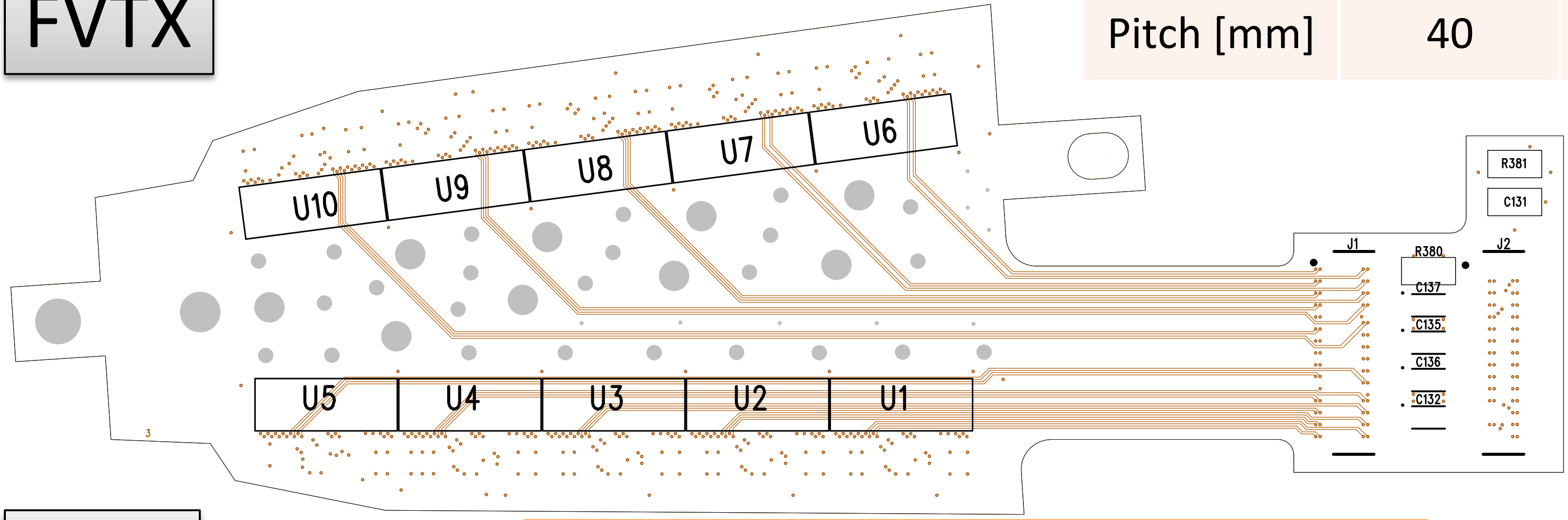
# INTT System



# HDI Design

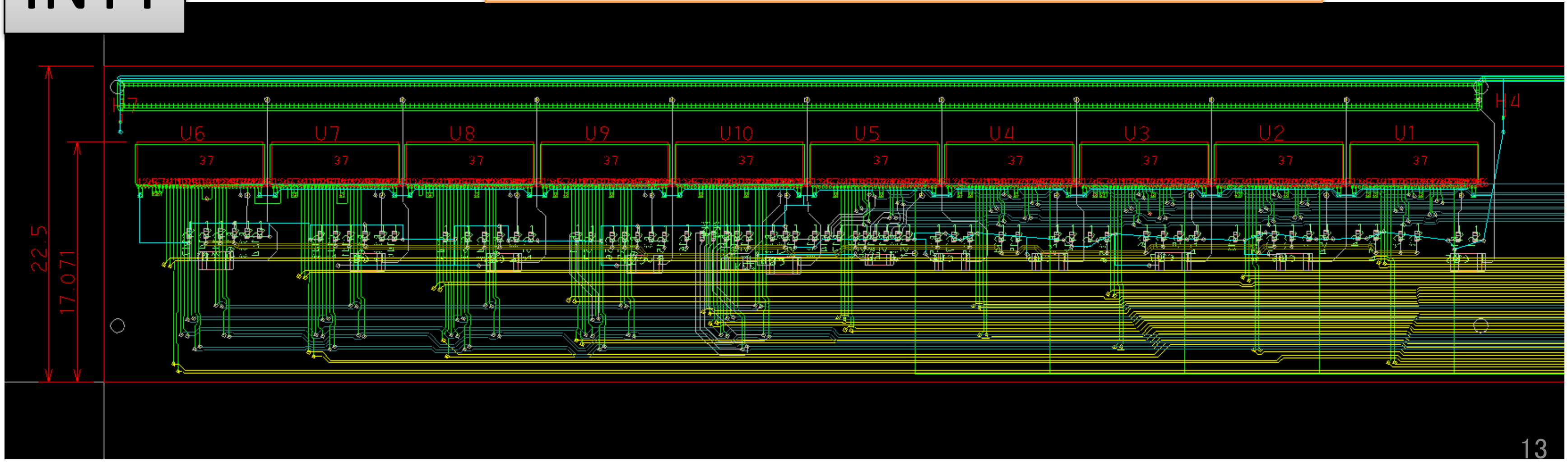
| | FVTX | INTT |
|---|---|---|
| # Layers | 7 | 7 |
| Pitch [mm] | 40 | 60 -> ? |

FVTX




Different Shape, but electrically same design.

INTT



# Collaborating Institutes and Expertise

- **RIKEN (Y. Akiba, I. Nakagawa)**
  - Conducted the PIXEL detector for PHENIX. In charge of design work and procurements of silicon sensors and HDIs with Japanese companies.
- **RBRC (T. Hachiya, G. Mitsuka,Y. Yamaguchi)**
  - Assembly and testing silicon module. Physics simulation and configuration optimization. Adapt FVTX readout electronics.
- **BNL (J. Huang, M. Lenz, E. Mannel, R. Nouicer, R. Pisani)**
  - Engineering and assembly of the ladder and support structures.
- **Rikkyo (H. Masuda)**
  - FPGA coding in readout electronics and slow controls and testing prototypes.
- **Nara Woman's University (M. Shimomura)**
  - Testing prototypes and productions.
- **LANL (M. Brooks, M. Liu)**
  - Played leading role in FVTX detector development. Consultant for the application of FVTX electronics to INTT.
- **J-Parc (S. Hasegawa, H. Sako)**
  - Additional funding and co-development of silicon sensors.

*FVTX expert

# R&D Schedule JFY2016

| 2016 Month | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 | 4 | Resource | Design |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| s1 Prototype-I | | | | | | | | | | | | | | | Production |
| Silicon Sensor | | | | | | | | | | | | | | RIKEN | Test |
| HDI | | | | | | | | | | | | | | RIKEN | |
| Silicon Module | | | | | | | | | | | | | | RBRC | |
| | | | | | | | | | | | | | | | |
| s0 Prototype-I | | | | | | | | | | | | | | | |
| Silicon Sensor | | | | | | | | | | | | | | RIKEN | |
| HDI | | | | | | | | | | | | | | RIKEN | |
| Silicon Module | | | | | | | | | | | | | | RBRC | |

Today

# Summary

- Intermediate tracker to improving the tracking performance in high multiplicity circumstance
- Similar design to PHENIX FVTX detector.
- Minimum technical challenge to be in time for day-1 experiment.
- Maximum use of existing FVTX readouts to reduce the cost.

# BACKUP SLIDES

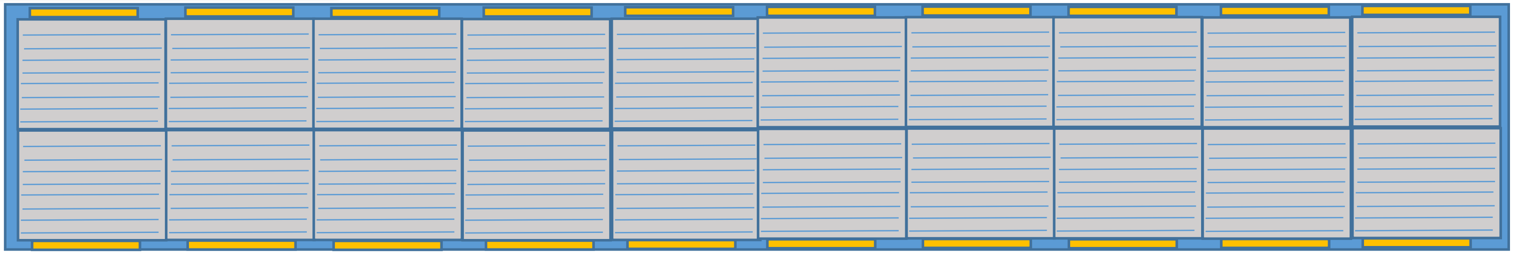
# s0 Sensor Design

## Silicon Cell

| Number of Strips | 128 |
|---|---|
| Strip  width | 84  um |
| Strip length | 12 mm |

| Block Width | 128 × 84 um = 10.752 mm |
|---|---|
| Block Length | 12 mmm |

## Silicon Sensor



| Number of Blocks | 12 × 2 =24 |
|---|---|
| Active Are | (2 × 10.752) mm  × (12 × 10) mm |

Design by Yasuyuki Akiba

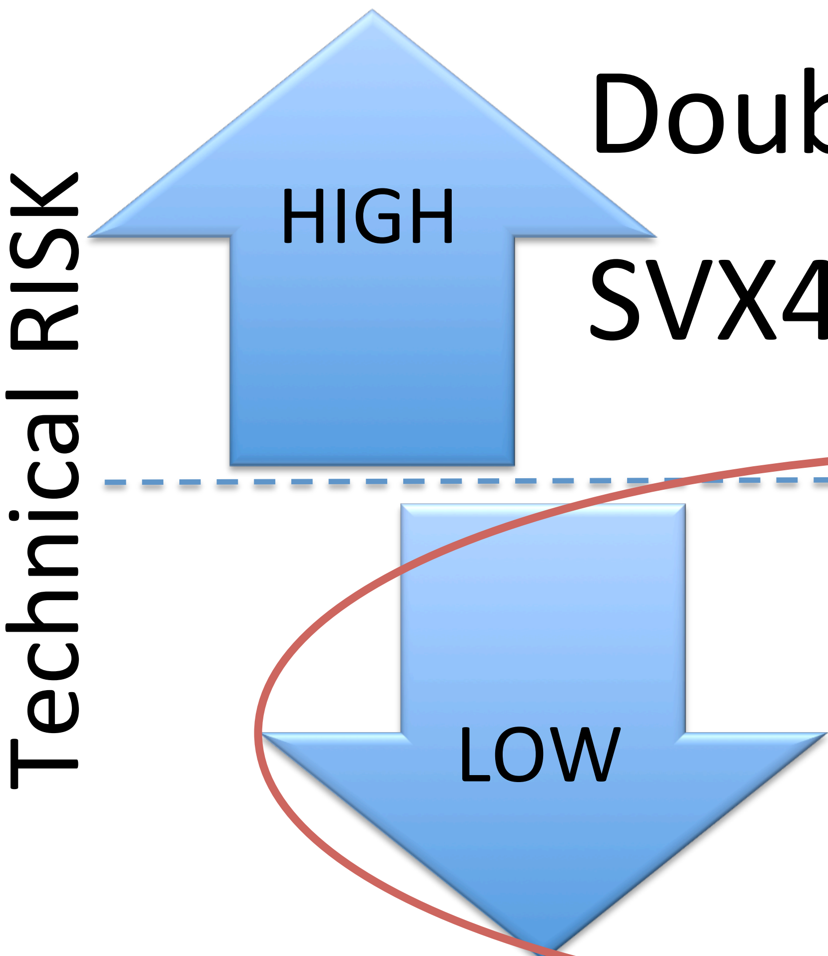
# Managements

- Project manager (Itaru Nakagawa)
- deputy manager (Rachid Nouicer)
- Subsystem managers
  - Detector assembly and construction (Rachid Nouicer)
  - Mechanical and integration (Rob Pisani)
  - Electronics and readouts (Eric Mannel and Takashi Hachiya)
  - Software (Gaku Mitsuka)
  - LV + HV and Slow control (Yorito Yamaguchi)

# Outline

- Role of the intermediate tracker (INTT)
- INTT concept
  - Configuration
  - Technology
  - Cost

# Technological Choice




Double sided sensor

SVX4 chip

Single sided sensor

FPHX chip

# Collaboration

- RIKEN (Y. Akiba, I. Nakagawa)
- RBRC (T. Hachiya, G. Mitsuka,Y. Yamaguchi)
- BNL (J. Huang, M. Lenz, E. Mannel, R. Nouicer, R. Pisani)
- Rikkyo (H. Masuda, Kazu Kurita?)
- Nara woman's university (M. Shimomura)
- LANL (M. Brooks, M. Liu)
- New Mexico (D. Field*)
- J-Parc (S. Hasegawa, H. Sako)
- Tsukuba (S. Esumi)

*FVTX expert

# Basic Project Philosophy

# Basic Design Philosophy

## Technology

- Employ existing technology
- Employ technology we are familiar with

## Man Power

- Collaborate with Institutes which have the experience and infrastructure

## **Minimum Cost**

- Little "R" and rather focus on "D"
- As compact as possible

## Schedule

- **To be in time for 2022**